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219.40780X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

5/ Letter re. IDS
E. Willis
8-21-02

Applicant(s): B. CHANDRAN ET AL.

Serial No.: 10/023,723

Filed: December 21, 2001

For: SEMICONDUCTOR PACKAGE WITH LOW RESISTANCE PACKAGE-TO-DIE INTERCONNECT SCHEME FOR REDUCED DIE STRESSES

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.97 & §1.98

Assistant Commissioner of Patents
Washington, D.C. 20231

January 18, 2002

Sir:

The Examiner's attention is directed to commonly assigned, copending application, Serial No. 10/023,819 by the same inventors as the above-identified application, entitled "Chip-Join Process to Reduce Elongation Mismatch Between The Adherents And Semiconductor Package Made Thereby".

Respectfully submitted,

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